

FIG. 1

FIG. 2 is a cross-sectional view of a semiconductor device, taken along line 2-2 of FIG. 1, showing a top view of the device. The device includes a substrate 100, a gate stack 102, and a source/drain region 104. The gate stack 102 is formed on the substrate 100 and includes a gate dielectric layer 106 and a gate electrode layer 108. The source/drain region 104 is formed in the substrate 100 and includes a source/drain dielectric layer 110 and a source/drain electrode layer 112. The device is shown in a cross-sectional view, with the gate stack 102 and source/drain region 104 being the main components. The gate stack 102 is formed on the substrate 100 and includes a gate dielectric layer 106 and a gate electrode layer 108. The source/drain region 104 is formed in the substrate 100 and includes a source/drain dielectric layer 110 and a source/drain electrode layer 112. The device is shown in a cross-sectional view, with the gate stack 102 and source/drain region 104 being the main components.

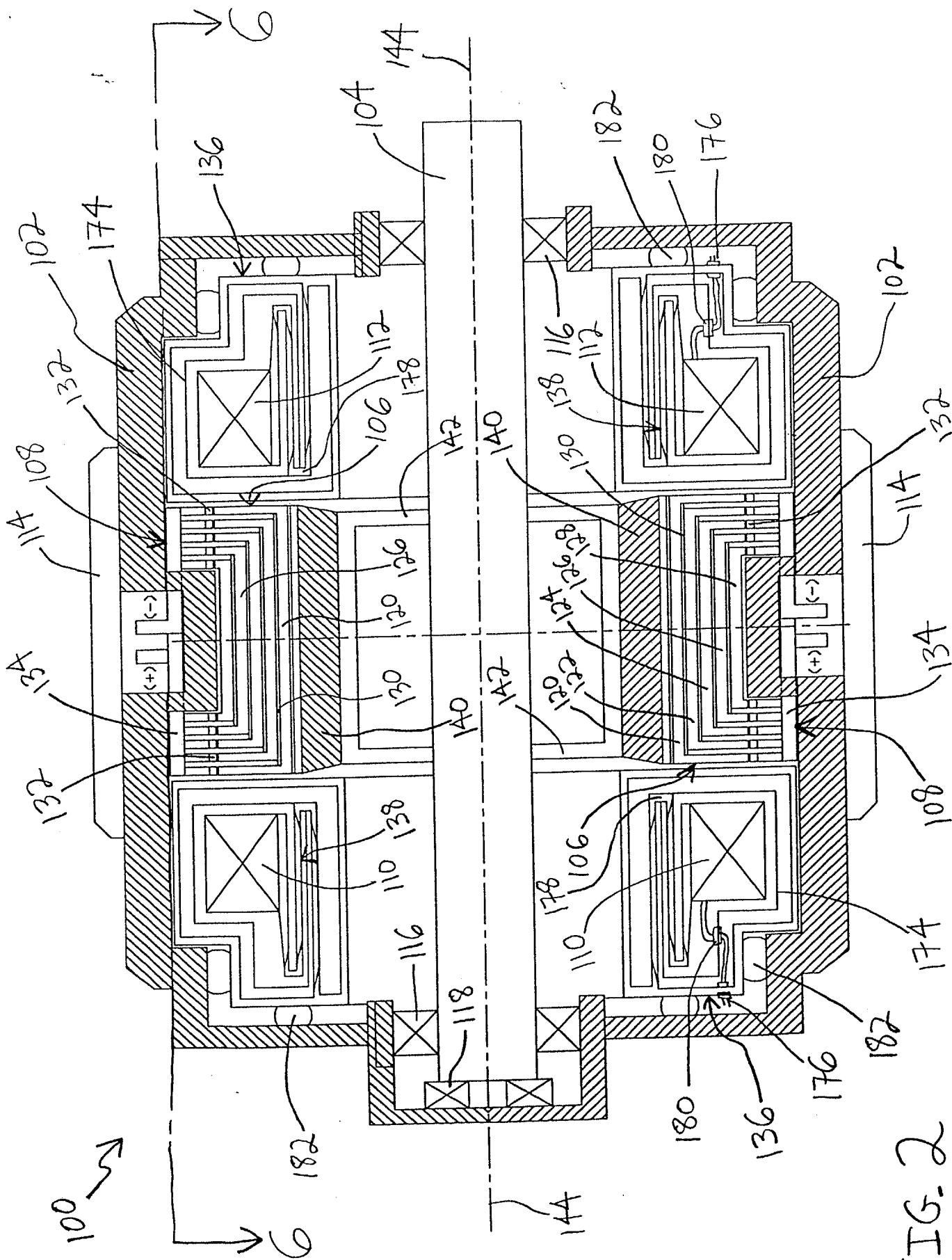


FIG. 2

FIG. 3

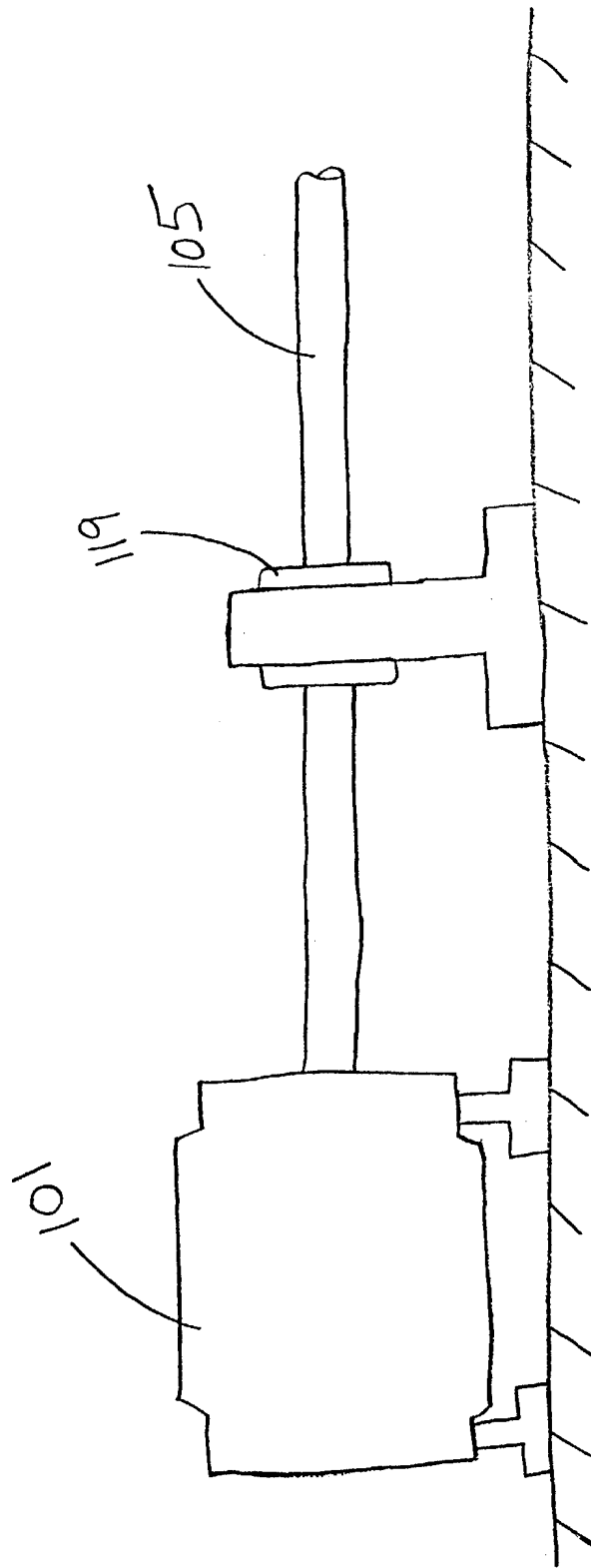


FIG. 3

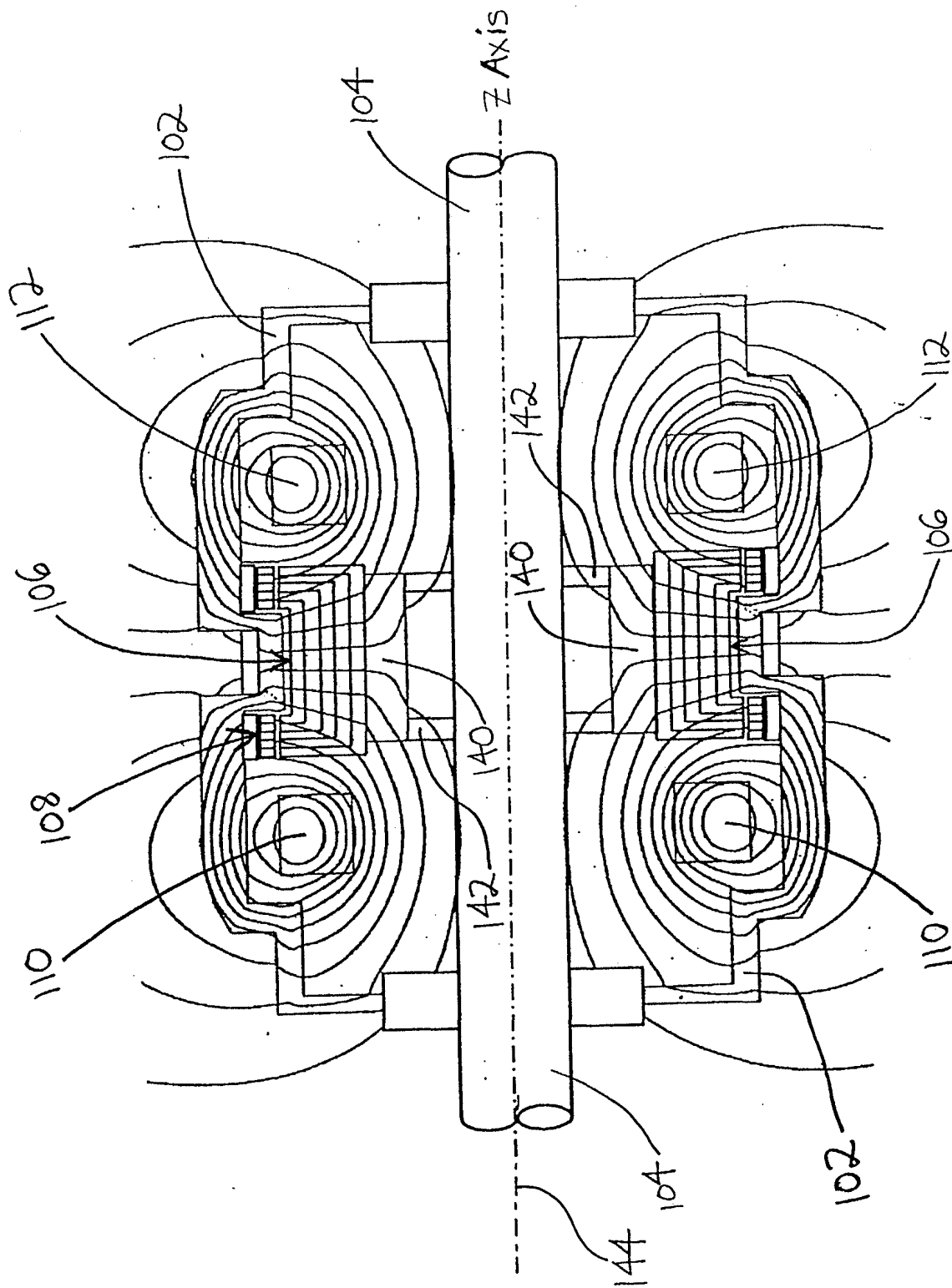


FIG. 4

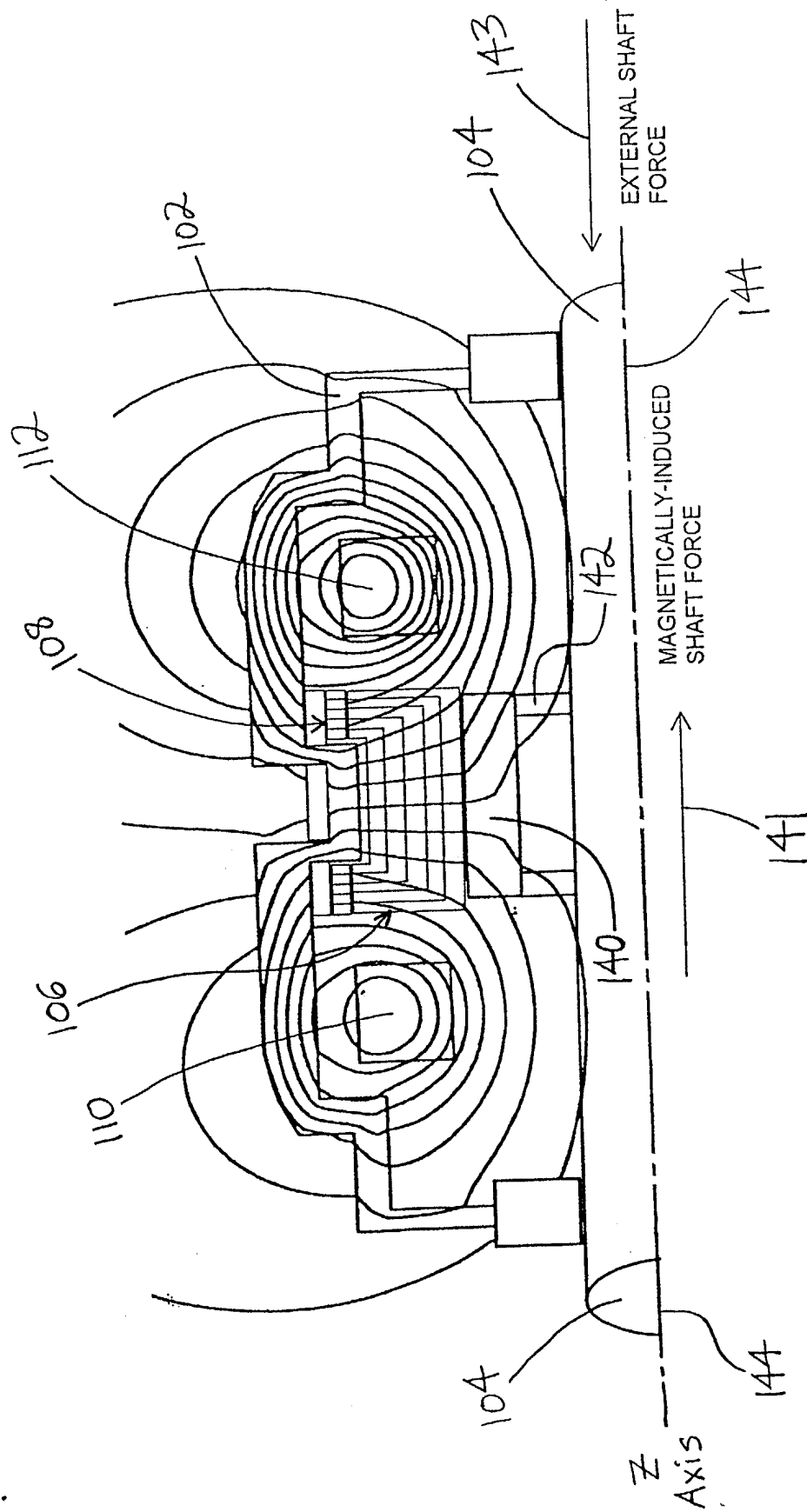


FIG. 5

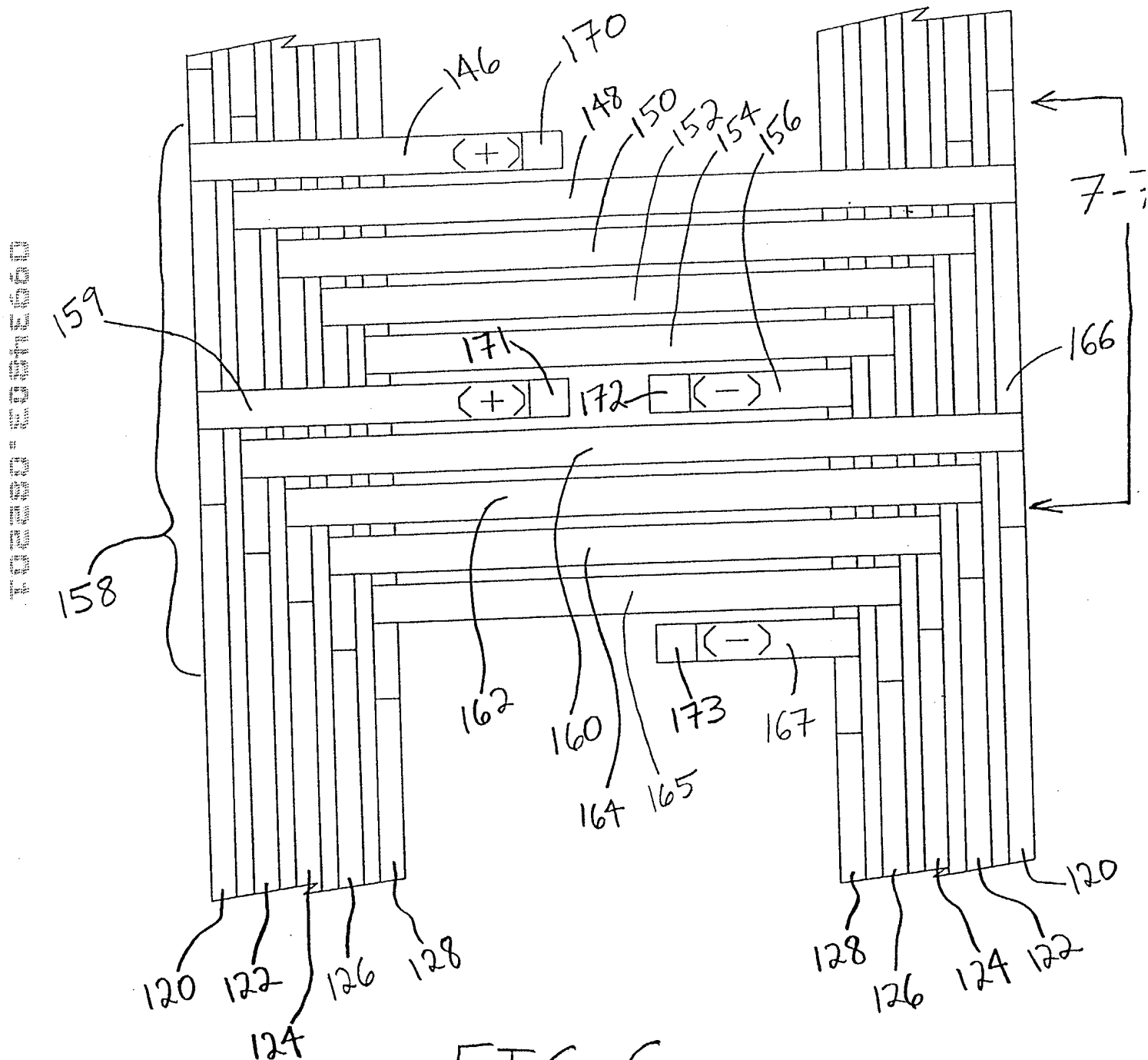


FIG. 6

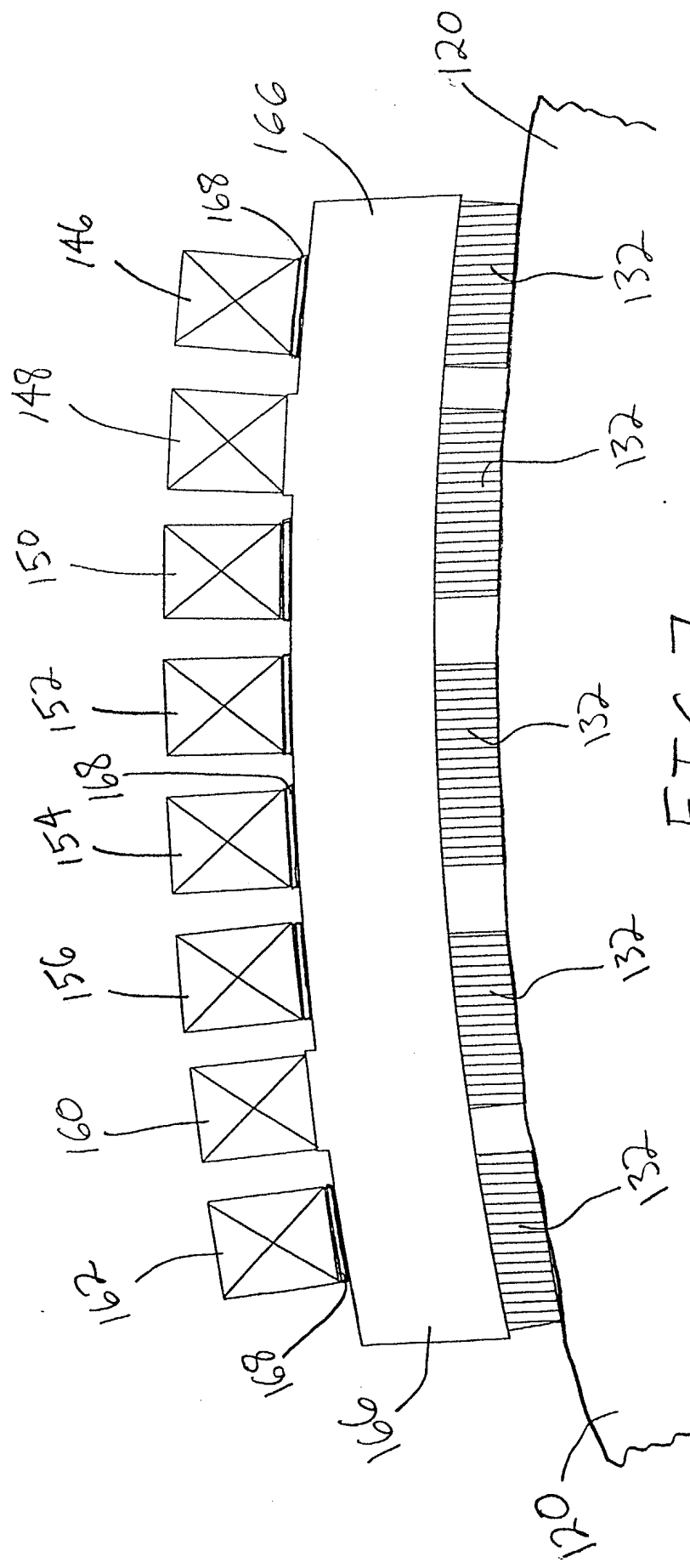


FIG. 7

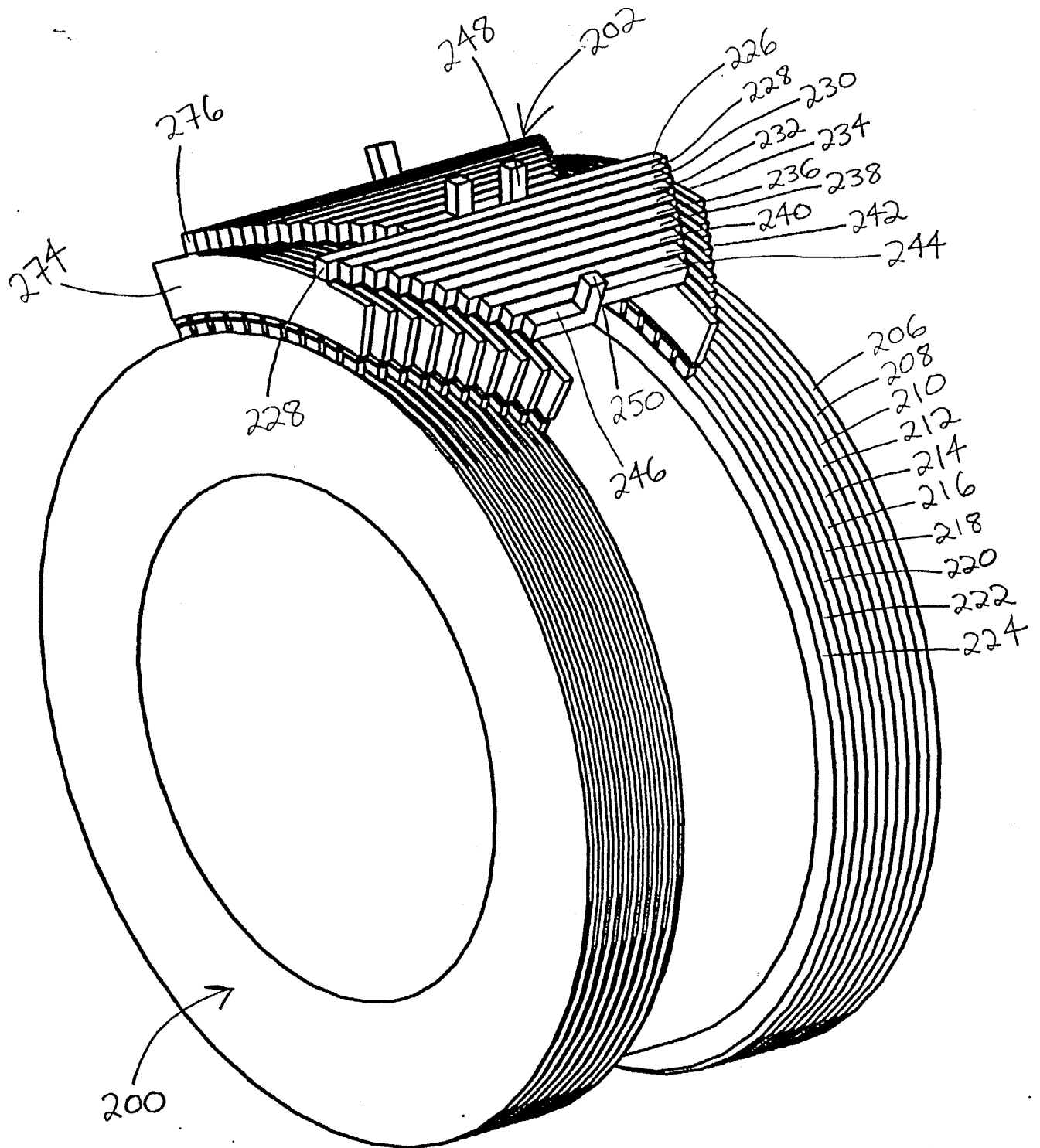
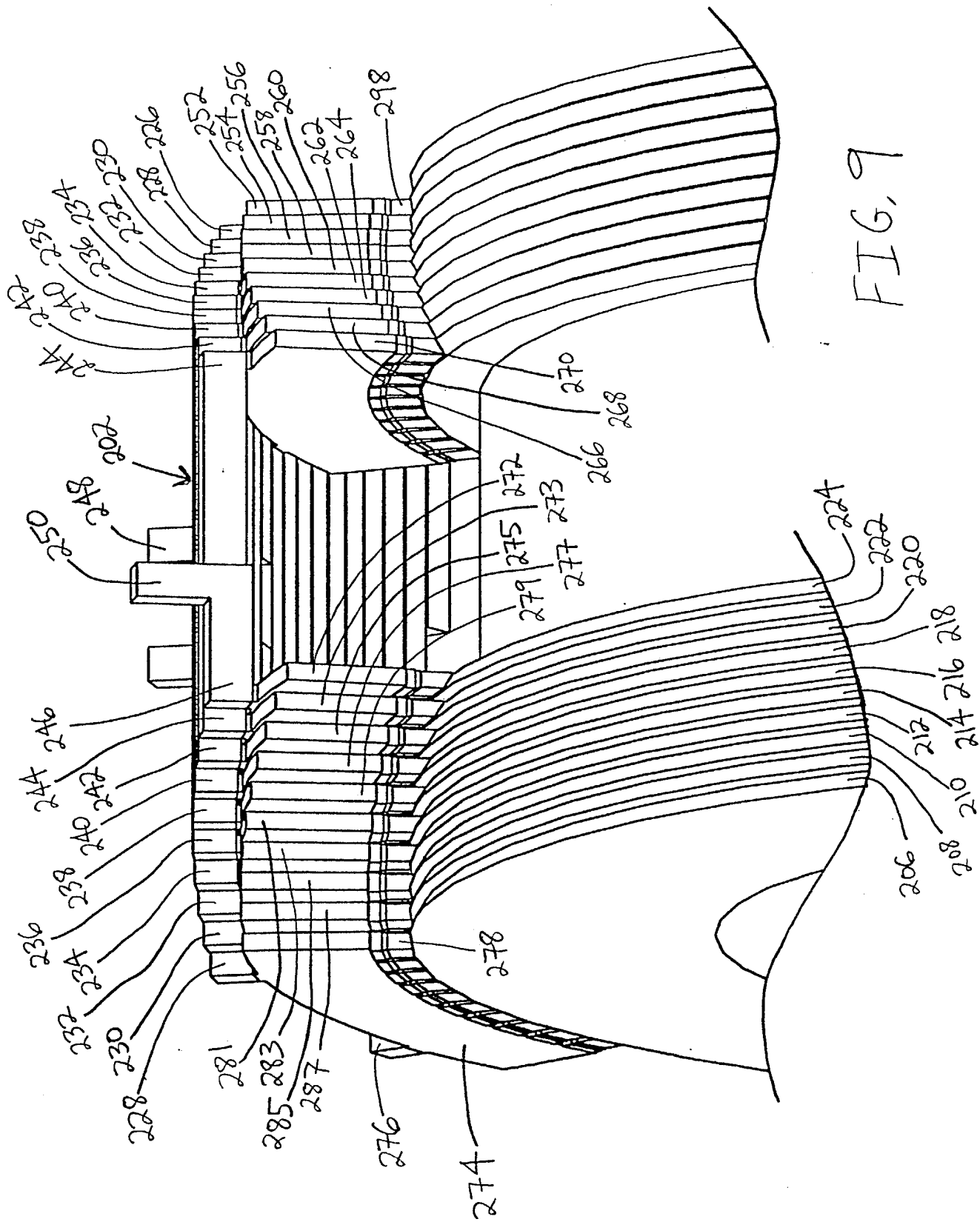


FIG. 8





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FIG. 10 is a perspective view of the device 100 in a closed position.

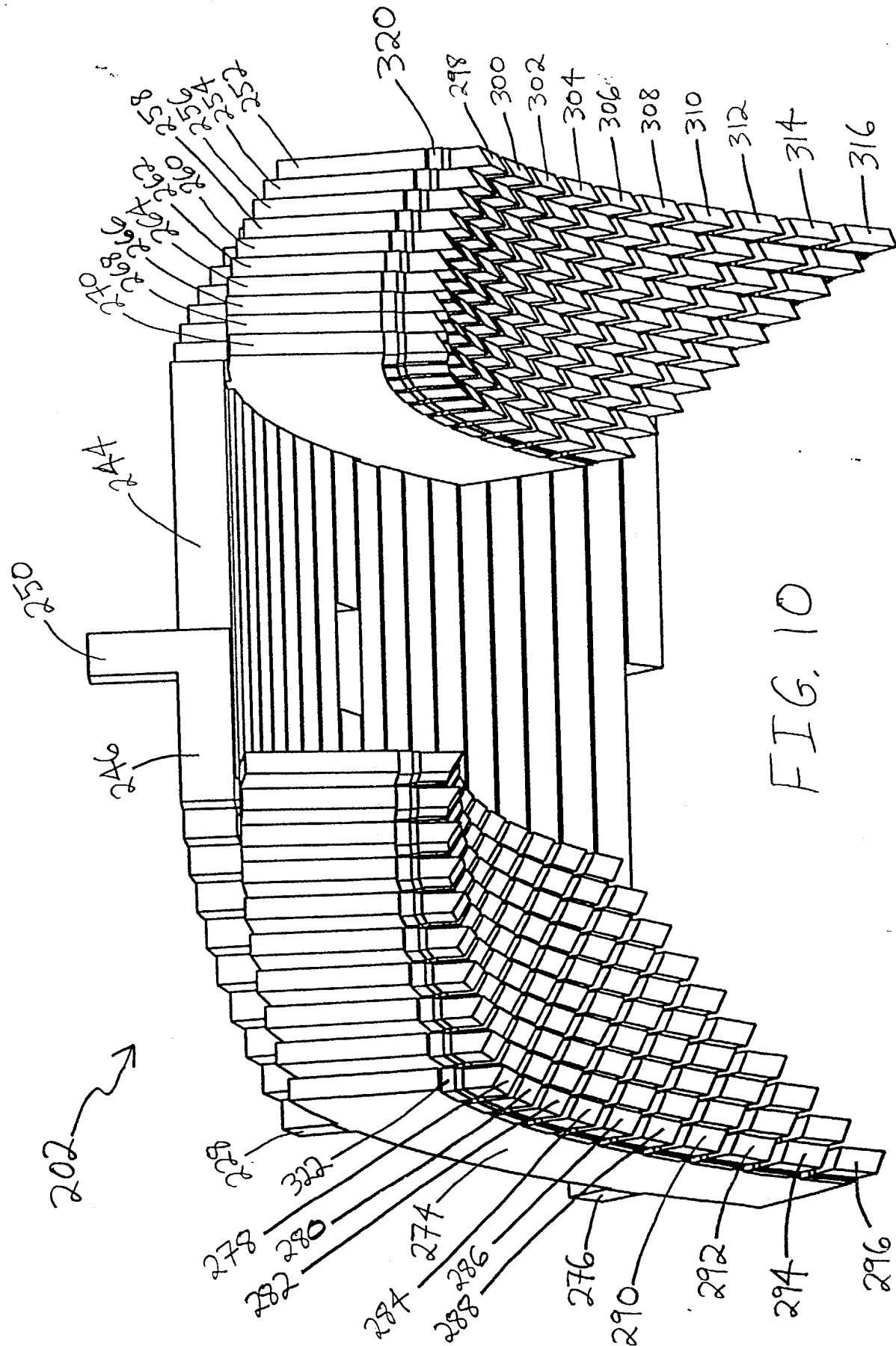


FIG. 10